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Design and Power Evaluation of Low Power DET-STSFF

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Abstract

In this Paper, a new design of Flip-Flop has proposed, having a structure of explicit Dual Edge pulse-triggered with a modified True Single Phase Clock (TSPC) latch based on signal feed through scheme. The performance of Dual Edge Triggered-Signal feed Through Scheme Flip-Flop(DET-STSFF) is analyzed and compared with that of two different types of Flip-Flops(FF) based Adapative Coupling Element(ACE) Scheme and Semidynamic based Flip-Flop is designed using Tanner EDA Tool based up on 0.25µm CMOS Technology. The performed is analyzed through simulation of Flip-Flops using T- SPICE, L-EDIT, S-EDIT tools of Tanner EDA Tools. The parameters of power consumption, Area, Delay, and Power Delay Product (PDP) are evaluated to analyze the proposed Low Power DET-STSFF.

Keywords: Adaptive Coupling Element (ACE), Complementary Metal Oxide Semiconductor (CMOS), Dual Edge Triggered-Signal feed Through Scheme FF (DET-STSFF), Flip-Flop (FF), Tanner.

Introduction

The Scaling of Complementary Metal Oxide Semiconductor (CMOS) Technology has improves the speed of the circuit, low cost and reduces area of the circuit. The Integrated Circuits, Microcontroller, Microprocessor are constructed from CMOS logic which reduces the power consumption and more immune towards noise occurring conditions. CMOS Technology scaling through nanometer regime causes the transistor parameter such as threshold voltage, channel length, mobility and oxide thickness to have large statistical process. The power-delay product (PDP) metric relates the amount of energy spent during the realization of determined task, and it stands for the more fair performance metric when comparing optimizations of a module designed and tested using different technologies, operating frequencies.

Fundamental Circuit required for Microprocessor is Flip-Flop (FF). FF is having two stages, one is Clock System and another is Latch system or data storage. Clock System consumes 50% more than total power of Chip. To overcome this problem a triggered based Flip-Flop is implemented. Flip-Flop is used to design counter, Register and Integrated Circuits. The PDP exhibited by the flip-flop would affect the system's overall performance. Taking this fact into consideration, the design in the flip-flop with low power dissipation and low propagation delay which improves the modern digital design to greater extent.

The power consumption is critically important in modern VLSI circuits especially for low-power applications. The power optimization techniques are applied at different levels of digital design. However, optimization at the logic level is one of the most important tasks to minimise the power. The logic components, latches and flip-flops are critical to the performance of digital systems. In particular, D type flip-flop (DFFs) are widely used in memory design and test applications. There are some concerns in the design of DFF such as $T_{D\text{-}Q}$ (the delay from the edge of Data to output of DFF) , C_L (load capacitance of the flip-flop clock), and the area. These parameters along with the clock frequency and the power consumption of the flip-flop determine the overall performance of a DFF. Reducing C_{clk} or the frequency of the clock has a great impact on the dynamic power consumption of the flip-flop clock tree.

Power dissipation is most sensitive parameter and it is classified in to dynamic and static power dissipation. Dynamic power dissipation occurs whenever circuit is operational, while static power dissipation it becomes an issue when the circuit is inactive or is in a power-down mode. There are three

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powers which are summarized in equation given below.

$P_a = P_{swt} + P_{sc} + P_{lek} = (\beta * V_{dd}^2 * C_L * f_{clk}) + (V_{dd} * I_{sc}) + (V_{dd} * I_{lek})$

The first term represents the switching component overpower, where C_L is the load capacitance, f_{clk} is the clock frequency and is the probability that a power consuming transition occurs (the activity factor). The second term due to the direct-path short circuit current, which arises when both the PMOS and NMOS transistors are simultaneously active, conducting current directly from V_{dd} to ground. Finally, leakage current, I_{lek} which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology.

The data activity rate β presents the average number of output transitions per clock cycle. As the total power dissipated in the flip-flop depends on the data activity, an illustration of power dissipated at data activities of 0%, 25%, and 100%. Data activity of 25% corresponds to 11001100... data pattern and 100% data activity corresponds to data pattern 101010... and so on. In order to analyze the performance of the flip-flop in the absence of any data switching, power dissipation corresponding to 0% data activity for 11111... and 00000…data patterns are provided. As mentioned earlier, the small precharge node, CLK-input, and data-input capacitances makes the proposed flip-flop power efficient at higher data rates.

In this Paper we report the design and comparison of Adaptive Coupling Flip-Flop (ACFF) and Semi dynamic Flip-Flop (SDFF). ACFF having feature of single phase clock structure with no clock buffer and no precharge stage, it provides more energy than Transmission Gate FF (TGFF) [4]. SDFF having pulse triggered generated (PG) circuit [1] which will increases the power consumption but PG Circuit can be shared to the group of FF's in Digital design which reduces overall power. The proposed Dual Edge Triggered Signal through Scheme Flip-Flop (DET-STSFF) are design by using a modified True Single Phase Clock (TSPC) Latch System and PG. The clock frequency is determined by system specifications, the use of dual edge-triggered flip-flops (DETFFs) can help to reduce the clock frequency to half that of the single edge-triggered flip-flops (SETFFs) while maintaining the same data throughput [7].

Existing Flip-Flops

Many of Low power Flip-Flops are discussed about Latch system and clock system. The different Flip-Flops ACFF, SDFF are designed and studied. The Existing Methodology ACFF is implemented having 22 transistors which is smallest transistor count. An adaptive coupling element (ACE) element is having one NMOS and one PMOS, configured in parallel and the gates are controlled by same data signal.

Figure 1 shows ACFF schematic, the simulation of this environment has been used for Flip-Flop analyses within the addition of the inverters at the outputs.

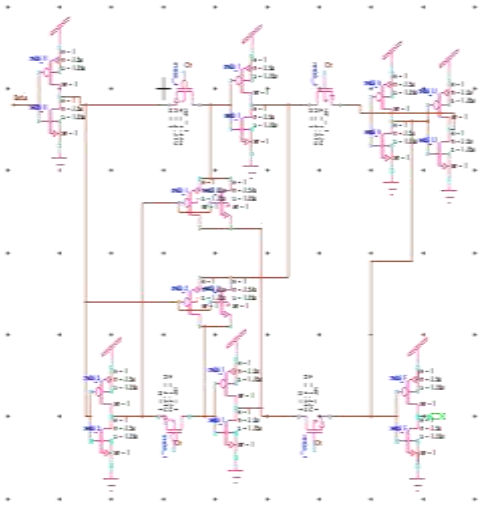

Figure 1: Schematic Design of ACFF

To reduce the pipeline, a new family of edge-triggered flip-flops has been developed. This FF's belongs to semidynamic and dynamic circuits that can interface to both static and dynamic logic. The main feature of basic design is small clock load, small area, short latency and a single-phase clock scheme. Semi dynamic Flip-Flop (SDFF) is integration of True single-phase clock (TSPC) latch and Pulse Generator (PG). TSPC latches can be combined in several different ways to implement edge-triggered flip-flops [1]. While their single clock phase is advantageous, a drawback of TSPC flip-flops is long latency. A way to reduce latency is to clock a single transparent latch with a very narrow pulse. Here, SDFF is a type of Pulse-triggered FF (P-FF). P-FF's, are referred either implicit or explicit type based on the pulse generated. In Implicit type P-

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FF, PG is a part of latch design and no extra pulse signal is required.

In Explicit P-FF, PG and Latch are separate and the pulses need to be generated externally. Implicit P-FF has a problem of long discharge path but economical in terms of power. Explicit P-FF consumes more power but because of logic separation there is a speed advantage and this single pulse signal can be shared to group of FF's.

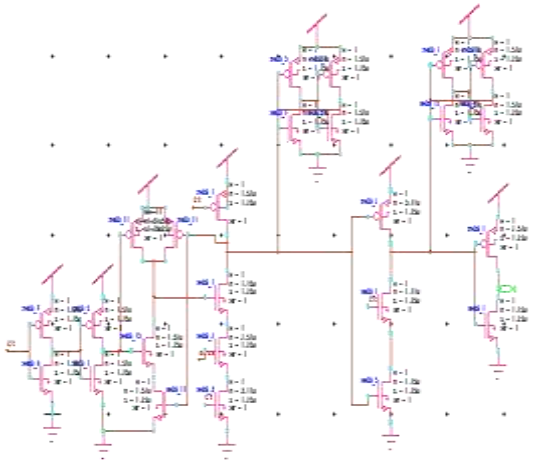

Figure 2: Schematic Design of SDFF

Conventional FF's

In the previous section the design is performed using schematic entry and same design is developed through layout format. In this simulation, the FF performance and comparisons regarding area, power consumption, delay and PDP. It consists of FF with 1.5v source, PMOS and NMOS transistors are width 2.50nm and 2.50nm width. The Figure 3 shows the ACFF layout design.

PMOS pass gates are too weak to pass through a substantially large drain current in order to overcome the strong coupling in state-retention circuitry during a transition. We introduce a new technique, the ACE, which configures ACFF such that the state-retention coupling is weakened if the input state is different to its internal state. This enables a transition to be performed easily, and allows ACFF to have a good tolerance to process variations.

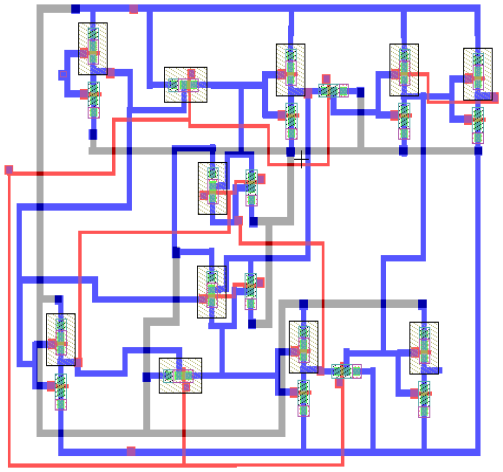

Figure 3: Layout Design of ACFF

Figure 4 shows SDFF layout design which consists of 25 transistors and this layout is designed for determining lowest power supply voltage, which each Flip-Flop can tolerate. One unique advantage of SDFF is that complex logic functions can be added easily. Indeed, most logic functions available in domino logic, such as wide or functions, multiplexors and complex gates can be implemented into SDFF [4].

Furthermore, this FF's family has the capability of easily construct logic functions with a small delay. This feature greatly reduces the pipelining, since each FF can be viewed as a special logic gate that serves as a synchronization element as well.

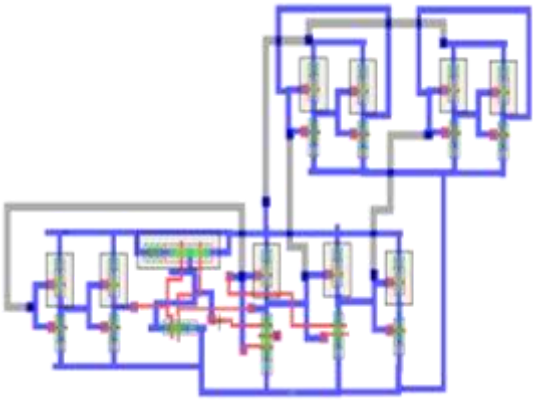

Figure 4: Layout Design of SDFF

DET-STSFF

The proposed work is implementation of Dual edge triggered Signal feed Through Scheme FF

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(DET-STSFF). By which exhibit static dissipation and this is the new DET-STSFF and SDFF which are implemented with logic style that have in-complement voltage swing resorted in some internal nodes, causing this consumption component. Which it was reduce Power delay product, Power, Area and delay. The power consumption improves the FF taken in descending order with optimizations power.

By using Modified True Single Phase Latch (TSPC) and Dual Edge PG [5] Based Flip-Flop it can provide low power with very efficiently optimizes its area. The implementation of this area obtained from layouts, it has been proposed for Flip-Flop requires the smallest area, which can also be considered has one factor for presenting low power consumption and delay for it implies smaller parasitic capacitance has been driven inside the Flip-Flop. The main reason for the smaller area compared to the other FF's that has been less transistors, is that size of the transistors in the proposed FF's.

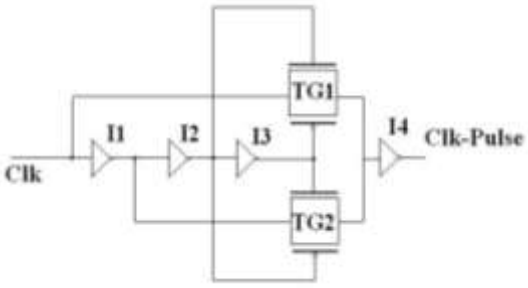

Figure 5: Dual Edge Triggered Pulse Generator

Modified True Single Phase Latch (TSPC) has mainly of three changes.

(i) Weak Pull up PMOS Transistor of Gate terminal is connected to Ground.

(ii) A pass transistor Controlled by the Pulse Clock is included so that input data can drive node Q of latch directly.

(iii) Pull -down network of second stage inverter is completely removed.

Total four transistors are removed from the keeper device and two NMOS transistors are removed which will improving the speed and reduces the delay. Pass transistor provide driving current to node Q during 0 to 1 transition and discharging node Q during 1 to 0 transition.

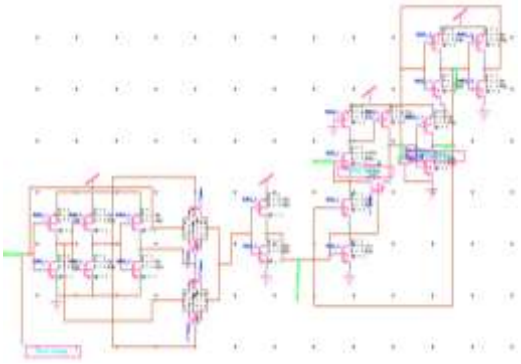

Figure 6: Schematic designed of DET-STSFF

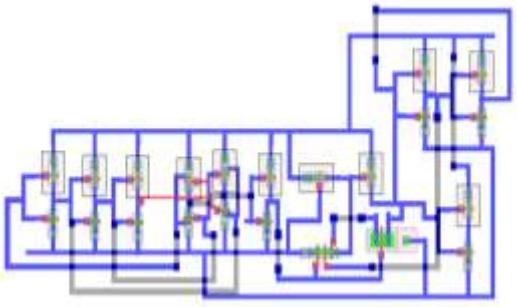

Figure 7: Layout Design of DET-STSFF

Simulation Results

By using S-Edit and L-Edit we have to calculate Power, Delay, Area and Power Delay Product (PDP). The operating condition used in simulations is 500 MHz/1.5 V. The output of the FF is loaded with a 20-pF capacitor. Considering the stimulation results the average delay for SDFF is 39.5ns and for ACFF is 40.117ns for comparing both when proposed DET-STSFF has the average delay is 36.343ns.The average Power for SDFF 0.44.83µW and ACFF has 25.25µW, by comparing the power proposed work has 18µW. The PDP for SDFF is 32.23fJ and for ACFF is 18.30fJ comparing both with proposed work DET-STSFF has the PDP is 7.97fJ.By using these values we have change in schematic capacitor values has C_L=20pF, V_{dd}=1.5v. Here, calculation of Power value for data 1011 with all Flip-Flops in this paper. Observation of PDP for different switching activities or data activities i.e., 100% (data=101010) 25% (data=11001100), 16.6% (data=111000) and 12.5% (data=11110000).The delay for SDFF is 7.19ns and for ACFF is 7.25ns by comparing both with DET-STSFF is 4.43ns.

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Table I Comparison of various FF's

	ACFF	SDFF	DET-STSFF
Layout Area(μm^2)	298.8	316.5	285.11
P_{avg}($\beta = 100\%$) (μW)	29.75	31.65	14.17
P_{avg}($\beta = 25\%$) (μW)	28.25	24.07	19.20
P_{avg}($\beta = 16.6\%$) (μW)	103.7	51.41	15.55
P_{avg}($\beta = 12.5\%$) (μW)	7.97	43.06	2.90

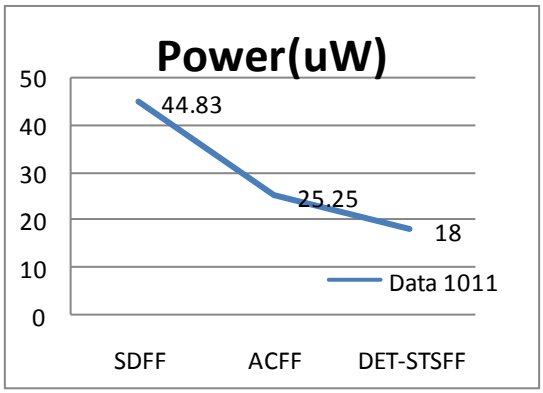

Figure 8: Power Chart

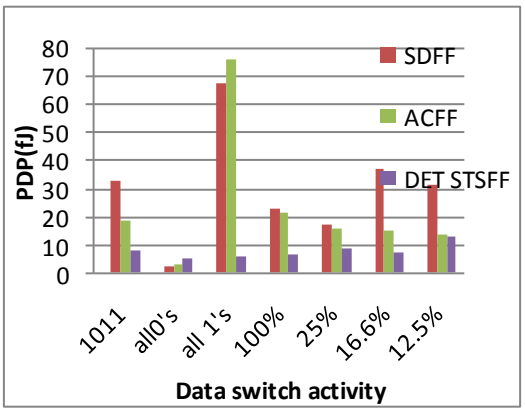

Figure 9: PDP Analysis

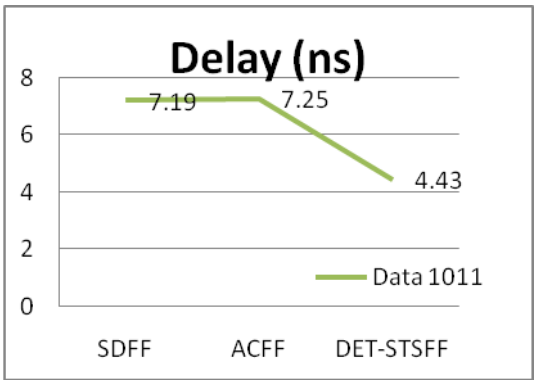

Figure 10: Delay Analysis

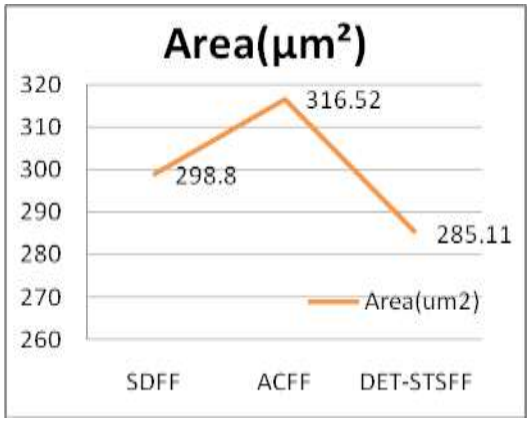

Figure 11: Area Chart

Conclusion

The paper presents design and implementation of DET STS Based Flip-Flop using which is most suitable for low-energy applications. Also the realization of DET-STSFF, the PDP improves by change of 56.44%, 75.27% with respect to ACFF and SDFF .The Power Consumption of DET-STSFF saving of 59.83%,28.71% with respect to ACFF and SDFF by using 0.25µm CMOS technology and thus flip-flops are implemented in real time applications like Counters, Registers, Microprocessors.

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